MMK200S160B

200A Thyristor Module

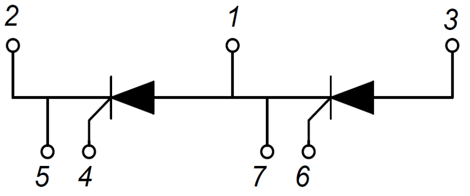
May 2015 Version 01 RoHS Compliant

PRODUCT FEATURES

- Electrically Isolated by DBC Ceramic
- High Surge Current Capability
- Low Inductance Package

APPLICATIONS

- DC Motor Control and Drives
- Battery Charges ,Heater controls,Light dimmers
- Static switches



ABSOLUTE MAXIMUM RATINGS

T_C=25°C unless otherwise specified

Symbol	Parameter/Test Conditions	Values MMK200S160B	Unit
V_{RRM}	Repetitive Peak Reverse Voltage	1600	V
V_{DRM}	Repetitive Peak Off State Voltage	1600	
V_{RSM}	Non-Repetitive Peak Reverse Voltage	1700	

Symbol	Parameter/Test Conditions		Values	Unit
$I_{T(AV)}$	Average On State Current	Single phase, half wave, 180°conduction, Tc= 80℃	200	A
$I_{T(RMS)}$	R.M.S. On State Current	Single phase, half wave, 180°conduction, Tc =80℃	310	
I_{TSM}	Non Repetitive Surge On State Current	1/2 cycle, 50HZ, peak value, Tc =45℃	5000	
		1/2 cycle, 60HZ, peak value, Tc =45℃	5400	
I^2t	For Fusing	1/2 cycle, 50HZ, peak value ,Tc =45℃	125.0	KA^2S
		1/2 cycle, 60HZ, peak value, Tc =45℃	121.0	
T_J	Junction Temperature		-40 to +125	℃
T_{STG}	Storage Temperature Range		-40 to +125	℃
V_{ISO}	Isolation Breakdown Voltage	AC, 50Hz(R.M.S), t=1minute	3000	V
Torque	Module to Sink	Recommended（M6）	3～5	Nm
Torque	Module Electrodes	Recommended（M6）	3～5	Nm
R_{thJC}	Junction to Case Thermal Resistance		0.12	K /W
Weight			160	g

ELECTRICAL CHARACTERISTICS

T_C=25°C unless otherwise specified

Symbol	Parameter/Test Conditions		Min.	Typ.	Max.	Unit
I_{DRM}	Maximum Peak Off-State Current	$V_D = V_{DRM}$, T_J = 125°C			25	mA
I_{RRM}	Maximum Peak Reverse Current	$V_R = V_{RRM}$, T_J = 125°C			25	
V_{TM}	Maximum on-state voltage drop	I_{TM}=600A,td=10 ms, half sine			1.75	V
V_{TO}	For power-loss calculations only	T_J = 125°C			0.85	V
r_T					1.7	mΩ
V_{GT}	Max. required DC gate voltage to trigger	V_A=6V, R_A=1Ω,T_J = -40°C			4.0	V
		V_A=6V, R_A=1Ω			2.5	
		V_A=6V, R_A=1Ω,T_J = 125°C			1.7	
I_{GT}	Max. required DC gate current to trigger	V_A=6V, R_A=1Ω,T_J = -40°C			270	mA
		V_A=6V, R_A=1Ω		75	150	
		V_A=6V, R_A=1Ω,T_J = 125°C			80	
V_{GD}	Max. required DC gate voltage not to trigger,$V_D = V_{DRM}$, T_J = 125°C				0.25	V
I_{GD}	Max. required DC gate current not to trigger,$V_D = V_{DRM}$, T_J = 125°C				10	mA
I_H	Maximum holding current			150	300	mA
I_L	Maximum latching current			250	500	mA
P_{GM}	Maximum peak gate power				10	W
$P_{G(AV)}$	Maximum average gate power				2.5	
I_{GM}	Maximum peak gate current				2.5	A
$-V_{GM}$	Maximum peak negative gate voltage				10	V
dv/dt	Critical Rate of Rise of Off-State Voltage,T_J=125°C,exponential to 67% rated V_{DRM}				1000	V/μs
di/dt	$V_D = 2/3V_{DRM}$,I_G = 0.3A, dig/dt=0.3A/μs, T_J = 125°C				150	A/μs

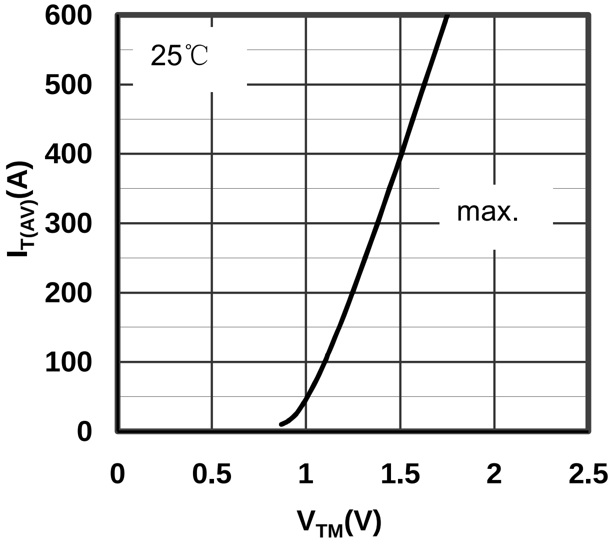


Figure 1. SCR Average On State Current vs Forward Voltage

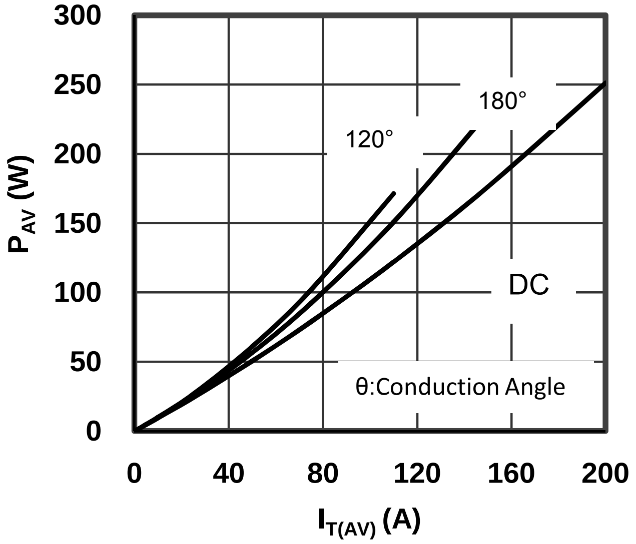


Figure2. SCR Power dissipation vs $I_{T(AV)}$

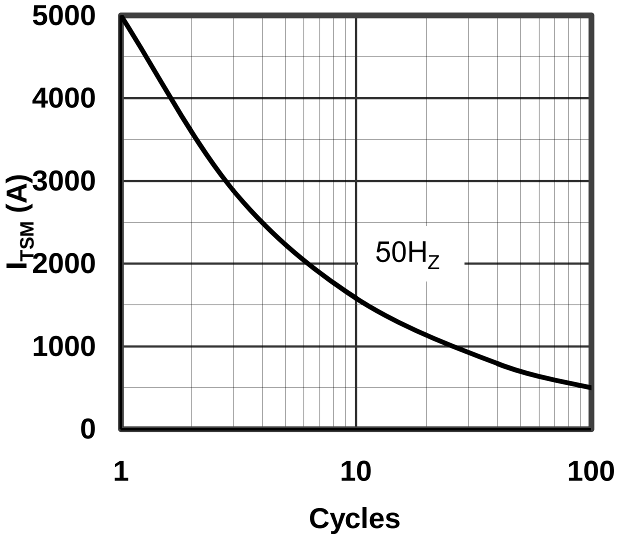


Figure 3. Max Non Repetitive Surge On State Current

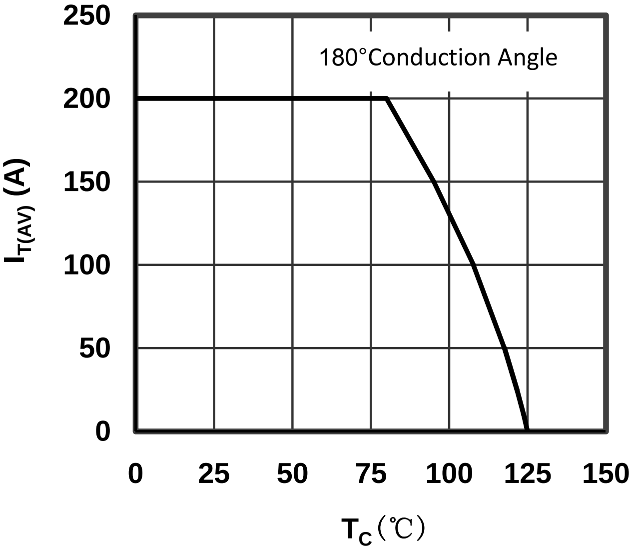


Figure 4. On State current vs Case temperature

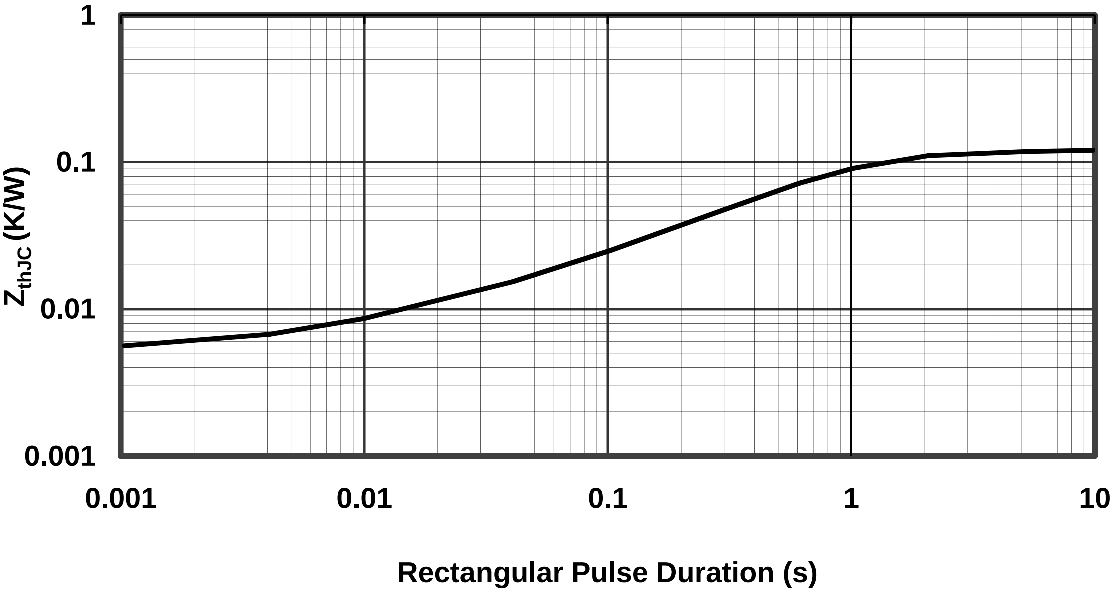


Figure 5. Transient Thermal Impedance

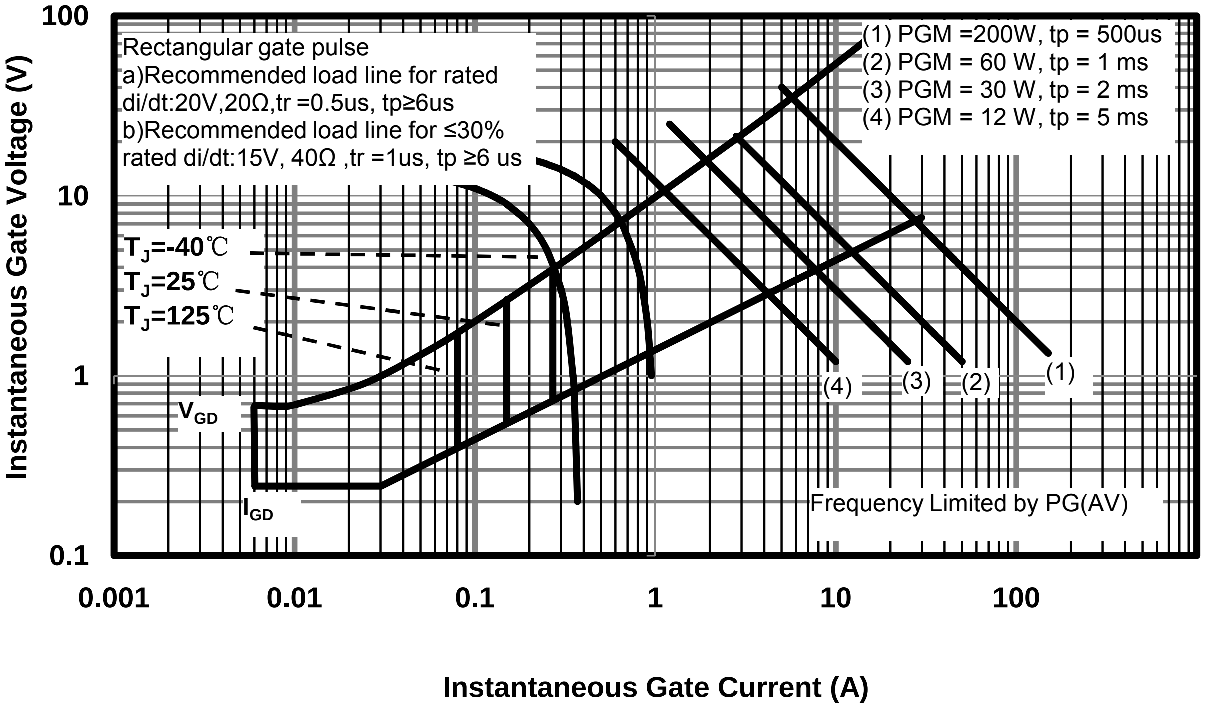
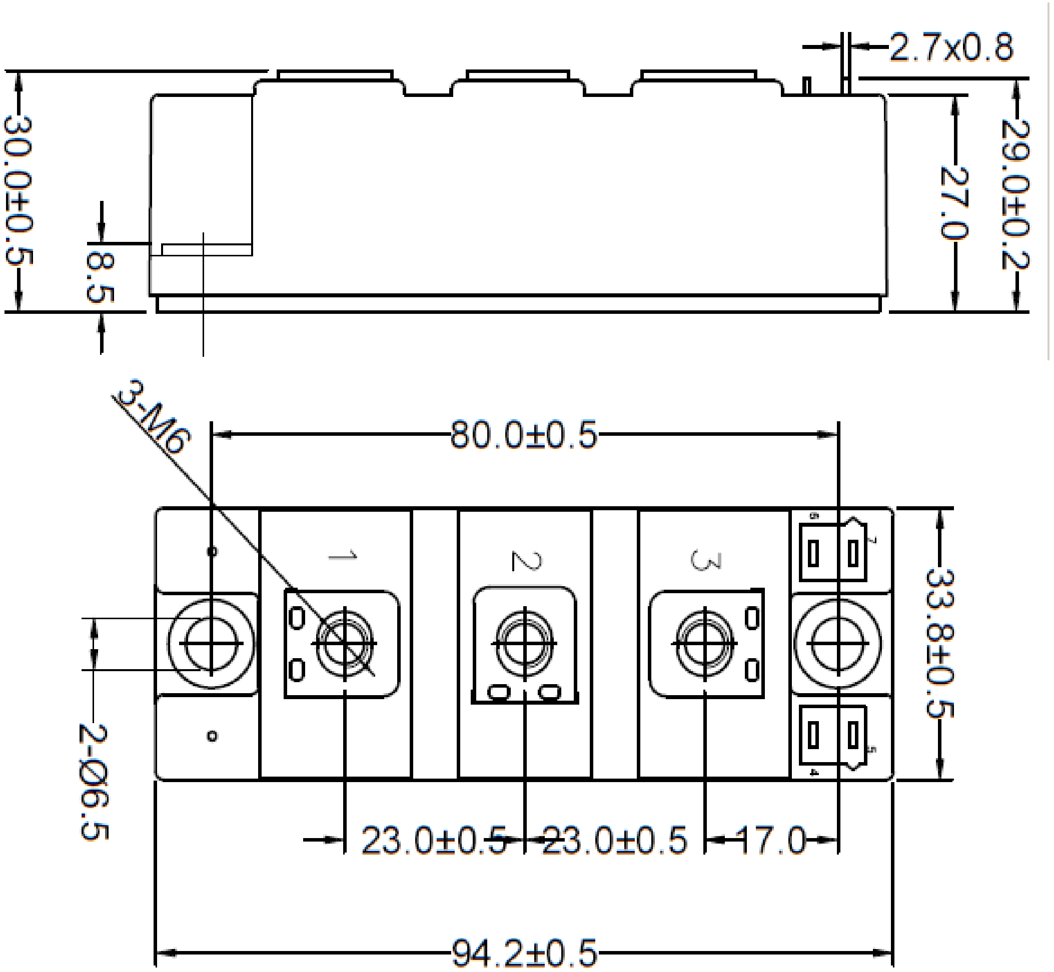


Figure 6. Gate Characteristics



Dimensions in (mm)

Figure 7. Package Outline